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EXAMINER	
WHITE, DYLAN C	

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,712	DROTTAR ET AL.	
	Examiner	Art Unit	
	DYLAN WHITE	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *2-5* is/are withdrawn from consideration.

5)☒ Claim(s) *11,16-19 and 24-26* is/are allowed.

6)☒ Claim(s) *1,6-10,12-15 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The Examiner acknowledges the cancellation of claims 2-5, addition of claims 24-26, and the amendments to the drawings.

Response to Arguments

Applicant's arguments filed 12/8/2007 have been fully considered but they are not persuasive.

The Applicant argues that the combination of Urakami and Arcoleo fail to disclose that of claims 1, 12, and 20. The Examiner respectfully disagrees because Urakami discloses where the second circuit (including transistors 21, 22, 27.1-n and 28.1-n) can be sized with respect to the first circuit (transistors 19 and 20) for adjusting characteristics of the output circuit.

The reference of Arcoleo discloses that it is well known to have adjustable circuits (impedance matching) to match the drive strength to the electrical load to reduce or eliminate signal reflections, voltage overshoot and undershoot and timing mismatch that can occur. Additionally Arcoleo includes where the size of a drive transistor can me modified by changes to transistor characteristics which include but are not limited to length, width, capacitance, and channel resistance. These changes would be obvious to one of ordinary skill in the art where N-type transistors can be larger than P-type transistors.

Furthermore MPEP 2144.04 IV teaches; A change is size is generally recognized as being within the level of ordinary skill in the art. Changing the physical size of the transistor does not change the overall functionality of the transistor or the inverter circuit (it may change the threshold voltage, turn on voltage, and saturation region of the transistor but it does not change the function of the transistor (switching on/off) or the function of the inverter (switching high to low)) and therefore is generally regarded as within the level of ordinary skill in the art. Therefore the case law as stated in 2144.04 IV does properly apply to the subject matter of claim 1.

Regarding Applicants arguments of equal rise and fall times on the output port, it is related the changing of size in the transistors. It is extremely well know in the art that changing the size of a transistor will effect the speed at which a transistor switches; larger transistors switch slower while smaller transistors switch faster and it is also well know in the art that equal size PMOS and NMOS transistors do not switch at the same speeds, therefore in changing the size of transistors and where the NMOS is larger than the PMOS it is possible through design choice and transistors sizing to determine where the transmitter would generate substantially equal rise and fall times.

Applicants arguments regarding dependent claims 6-10 and 12-15 are based on the response above as they are dependent claims on the independents.

Regarding claims 16-19, the Applicants arguments are moot in view of amendments to claim 16.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-10 and 12-15, are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakami et al. (U.S. Pat. 6,794,909) in view of Arcoleo et al. (U.S. Pat. 5,864,506).

Regarding claim 1, Urakami discloses a first circuit (transistors 19 & 20 @ Fig. 2) couple to an input port (input) of the transmitter (4 @ Fig. 2), the first circuit including an input port (gates of transistors 19 & 20) and an output port (at node N11) and an inverter (transistors 19 & 20) including no more than two transistors (19 & 20) including a first transistor (19) having a source/drain directly connected to a source/drain of the second transistor (20) and a first gate of the first transistor (gate of PMOS transistor 19) and a second gate of a second transistor (gate of NMOS transistor 20) coupled directly to the input (input) of the transmitter (4 @ Fig. 2), where the first transistor (19) and the second transistor (20) of the inverter includes a n-type MOSFET (20) connected in series with a p-type MOSFET (19) and a second circuit (transistors 21, 22, 27.1-n, and 28.1-n) including a second circuit input port (gates of transistors 21 & 22) to the output

port of the first circuit (node N11), the second circuit including an output port (node N12) coupled to the output port of the transmitter (output), where the first circuit (transistors 19 & 20) is sized with respect to the second circuit (transistors 21, 22, 27.1-n, and 28.1-n, second circuit is sized by turning on/off transistors in the pull-up/pull-down array 27.n & 28.n) such that for a pulse applied to the input port of the transmitter (input), the transmitter generates an output signal (@ output) having a rise-time and fall-time substantially equal (turning on and off transistors 27.1-n and 28.1-n will size the second circuit to produce an output signal having rise and fall times substantially equal at the output port).

Urakami fails to disclose where the second transistor (20) is larger than the first transistor (19).

Arcoleo discloses an output driver where the size of a transistor (501b) in an inverter (transistors 501a & 501b) can be selected based on the physical characteristics (col. 8, lines 20-26), where the N-type transistor can be about two to three times larger that the P-type transistor. Wherein the adjusting the size of the transistors effects the rise and fall time of the output signal based on the switching speeds of the NMOS and PMOS transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the output drive (transmitter) circuit as disclosed by Urakami with the transistor sizing as taught by Arcoleo for improved signal quality (by impedance matching) and timing adjustments based on transistor size.

Regarding claim 6, the combination discloses where the second circuit includes a plurality of driver circuits (Urakami, 27.1-n & 28.1-n @ Fig. 2).

Regarding claim 7, the combination discloses where each of the plurality of driver circuits (Urakami, Fig. 2) includes a p-type MOSFET (19, 21, 27.1-n) connected in series with an N-type MOSFET (20, 22, 28.1-n, respectively).

Regarding claim 8, the combination discloses where the P-type MOSFET (Urakami; 19 @ Fig. 2) is sized to source a first current (from VDD) and the N-type MOSFET is sized so sink a second current (to GND) substantially equal to the first current (the transistors have to be sized in order to handle substantially equal first and second currents, if the transistors were too small they would burn out).

Regarding claim 9, the combination discloses where the second circuit (Urakami, 21, 22, 27.1-n, and 28.1-n) is connected to an equalization control circuit (transistor controls for 27.1-n and 28.1-n).

Regarding claim 10, the combination discloses where the equalization control provides de-emphases (Urakami; col. 5, lines 19-26).

Regarding claim 12, Urakami discloses receiving a signal (at input @ Fig. 2) at a first circuit (transistors 19 & 20), the first circuit including an input port (input) and an

output port (at node N11) and no more than two transistors (19 & 20) including a first transistor (19) having a source/drain directly connected to a source/drain of the second transistor (20); a first gate of the first transistor (19 @ Fig. 2) and a second gate of the second transistor (20) both coupled directly to the input port of the transmitter (input); a second circuit (transistors 21, 22, 27.1-n, and 28.1-n) coupled to the first circuit (at node N11), the second circuit including a plurality of P-type MOSFET's (21, 27.1-n), enabling the plurality of P-type MOSFET's to drive a transmission line (connected to output); and enabling less than the plurality of P-type MOSFET's (via control signals 15.1-n) to drive the transmission line (not shown, connected to output). Where the first circuit (transistors 19 & 20) is sized with respect to the second circuit (transistors 21, 22, 27.1-n, and 28.1-n) such that for a pulse applied to the input port of the transmitter, the transmitter generates an output signal having a rise-time and fall-time substantially equal (turning on and off transistors 27.1-n and 28.1-n will size the second circuit to produce an output signal having rise and fall times substantially equal at the output port).

Urakami fails to disclose where the second transistor (20) is larger than the first transistor (19).

Arcoleo discloses an output driver where the size of a transistor (501b) in an inverter (transistors 501a & 501b) can be selected based on the physical characteristics (col. 8, lines 20-26), where the N-type transistor can be larger that the P-type transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the output drive (transmitter) circuit as disclosed by Urakami with the

transistor sizing as taught by Arcoleo for improved signal quality (by impedance matching) and timing adjustments based on transistor size.

Regarding claim 13, the combination discloses receiving a signal at a first circuit (transistors 19 & 20) includes receiving a digital signal (at input node).

Regarding claim 14, the combination discloses enabling the plurality of P-type MOSFET's (27.1-n) to drive a transmission line (at output node) includes enabling the plurality of P-type MOSFET's substantially simultaneously (enabling gate control signals).

Regarding claim 15, the combination discloses where enabling less than all of the P-type MOSFET's (27.1-n) to drive the transmission line (not shown, connected to output) comprises enabling less than all of the p-type MOSFET's substantially simultaneously (don't have to enable all PMOS transistors).

Claim 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakami et al. (U.S. Pat. 6,794,909) in view of Arcoleo et al. (U.S. Pat. 5,864,506) in further view of Marshall et al. (U.S. Pat. 6,876,224).

Regarding claim 20, Urakami discloses a first circuit (transistors 19 & 20) coupled to an input port (input) of the transmitter (Fig. 2); wherein the first circuit (transistors 19 & 20) includes an inverter (transistors 19 & 20) including no more than two transistors

including a n-type MOSFET (20) connected in series (Fig. 2) with an p-type MOSFET (19), a first gate of the n-type MOSFET and a second gate of the p-type MOSFET both coupled directly to the input port of the transmitter (input), a second circuit (transistors 21, 22, 27.1-n, and 28.1-n) including a second input port (coupled to node N11) coupled to an output port of the first circuit (node N11), the second circuit including a second circuit output port coupled (N12) to the output port of the transmitter (output), where the first (transistors 19 & 20) and second (transistors 21, 22, 27.1-n, and 28.1-n) circuits are sized such that for an input signal the transmitter generates and output signal with a rise and fall time substantially equal to the input signal (turning on and off transistors 27.1-n and 28.1-n will size the second circuit to produce an output signal having rise and fall times substantially equal at the output port).

Urakami fails to disclose where the n-type MOSFET is about two and about three times larger than the p-type MOSFET.

Arcoleo discloses an output driver where the size of a transistor (501b) in an inverter (transistors 501a & 501b) can be selected based on the physical characteristics (col. 8, lines 20-26), where the N-type transistor can be about two to three times larger that the P-type transistor. Wherein the adjusting the size of the transistors effects the rise and fall time of the output signal based on the switching speeds of the NMOS and PMOS transistors. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the output drive (transmitter) circuit as disclosed by Urakami with the transistor sizing as taught by Arcoleo for improved signal quality (by impedance matching) and timing adjustments based on transistor size.

The combination of Urakami and Arcoleo fails to disclose where a first and second processor transmit and receive signals respectively.

Marshall discloses drivers embodied in a system (col. 5, lines 54-55) with a first processor (Marshall; 604 left) and a second processor (604 right) where the transmitter (Urakami, Fig. 2) can transmit to a receiver (not shown, but obvious) through transmission line (Marshall; 602 @ Fig. 6), therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter disclosed by Urakami with the system taught by Marshall for impedance matching to a transmission line for improved signal quality.

Claims 21-23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Urakami et al. (U.S. Pat. 6,794,909) in view of Arcoleo et al. (U.S. Pat. 5,864,506) in view of Marshall et al. (US Pat. 6,876,224) in further view of Song (US Pat. 6,614,258).

Regarding claim 21, the combination discloses that of claim 20, but fail to disclose a specific type of processor.

Song discloses where a processor in a dynamic logic array can be a very long instruction word processor (VLIW, col. 9, line17), therefore, It would have been obvious to one of ordinary skill in the art at the time of invention to use the transmitter combination of Urakami and Marshall with the VLIW processor taught by Song for faster processing of more complex functions.

Regarding claim 22, where the second processor is a complex instruction set processor (CISC; Song, col. 9, line 16).

Regarding claim 23, the combination discloses an equalization control (Urakami, from nodes N15.1-n and N16.1-n @ Fig. 2) coupled to the second circuit (27.1-n & 28.1-n) to provide de-emphasis.

Allowable Subject Matter

Claims 11, 16, and 24-26 are allowed. The following is an examiner's statement of reasons for allowance:

Regarding claims 11 and 16, where the transmitter transmits at a signal level and the first circuit and the second circuit are coupled to a supply potential having a value of at least twice the signal level.

Regarding claims 17-19, as being dependent on claim 16.

Regarding claims 24-26, as being dependent on claim 11.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to impedance matching and/or equalization circuits.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dylan White/
Examiner, Art Unit 2819

/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2819